

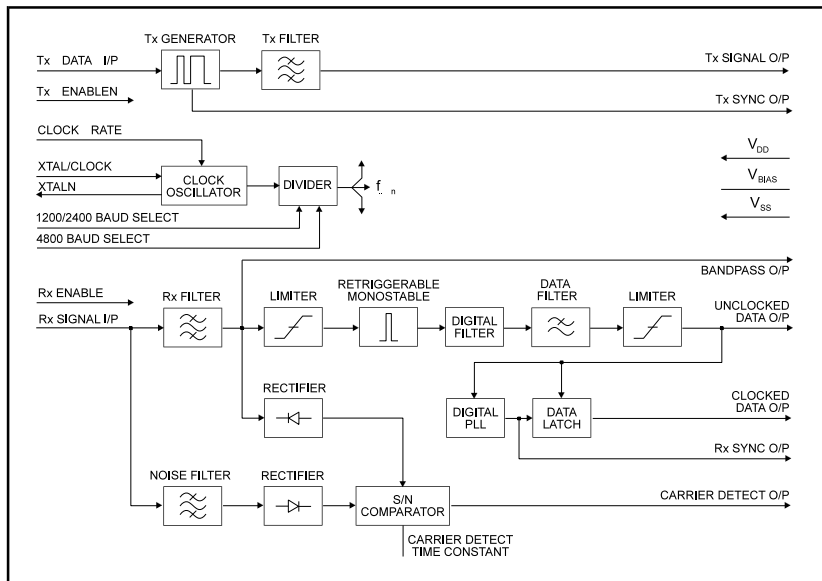
D/469A/3 June 2009

### Features

- Full-Duplex FFSK/MSK Modem with Separate Rx and Tx Enable Functions
- Pin Selectable Data Rates:  
*1200, 2400 or 4800 Baud*
- Pin Selectable Xtal/Clock Inputs:  
*1.008MHz or 4.032MHz*
- Clock Recovery Facility
- Carrier Detect Facility
- Low Power Operation (2.0mA typ. at 3.0V)

### Applications

- Data-Over Radio
- Personal/Cordless Telephone
- Radio and General Applications
- Narrowband Coax Data Channels
- Two Way Radio (MPT1327) Signalling
- Portable Data Terminals



### 1.1 Brief Description

The CMX469A is a single-chip CMOS LSI circuit which operates as a full-duplex 1200, 2400 or 4800 baud FFSK/MSK modem. The mark and space frequencies are 1200/1800, 1200/2400 and 2400/4800 Hz respectively. Tone frequencies are phase continuous; transitions occur at the zero crossing point. A common Xtal oscillator with a choice of two clock frequencies (1.008MHz or 4.032MHz) provides baud-rate, transmit frequencies, and Rx and Tx synchronization.

The transmitter and receiver operate entirely independently, including the individual section powersave functions. The CMX469A includes on-chip circuitry for Carrier Detect and Rx Clock recovery, both of which are made available as output pins. Rx, Tx and Carrier Detect paths contain bandpass filters to optimise signal conditions in each section of the modem. The CMX469A demonstrates good sensitivity and bit-error-rate under adverse signal conditions. The Carrier Detect time constant is set by an external capacitor, so that the product's performance can be optimised in high noise environments. This low-power device operates from a single supply between 2.7V and 5.5V, requires few external components and is available in a wide variety of plastic packages.

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### 1.2 Block Diagram

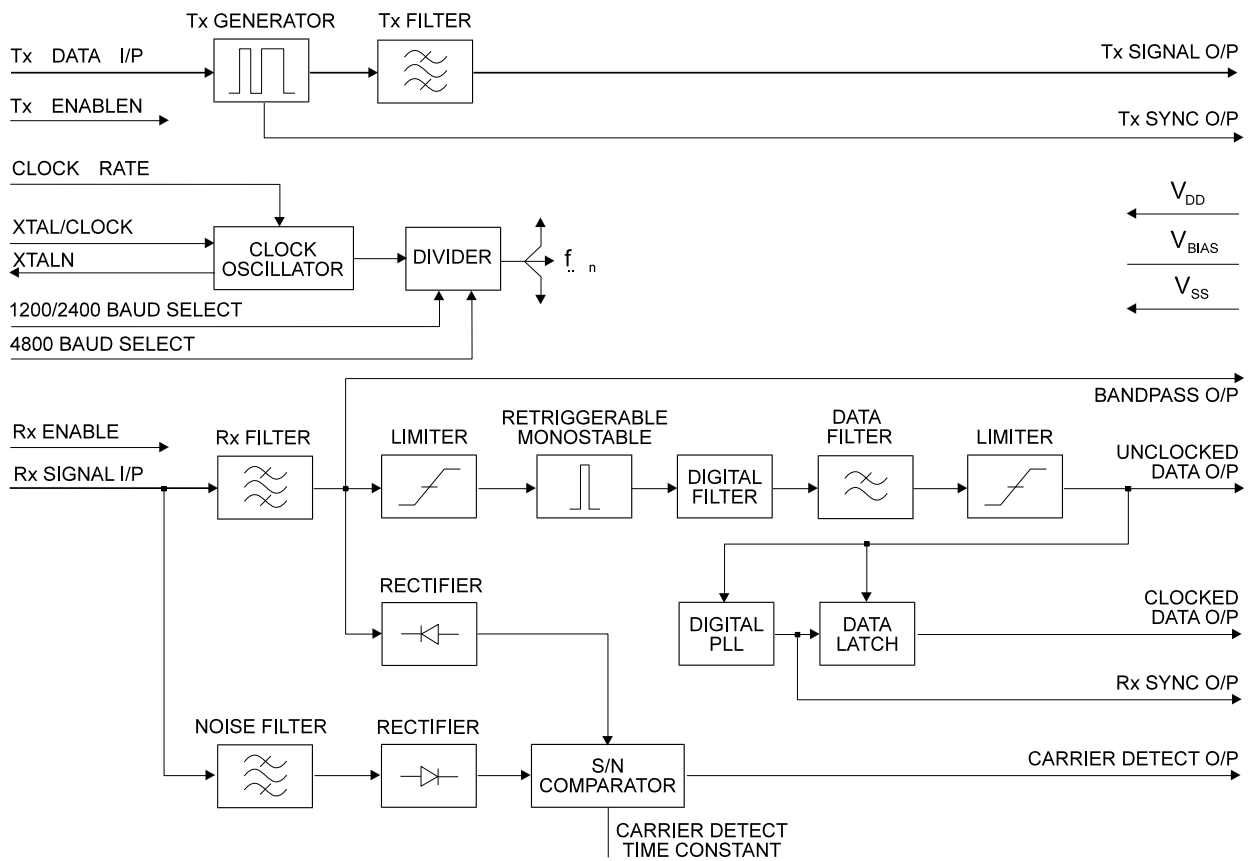


Figure 1 Block Diagram

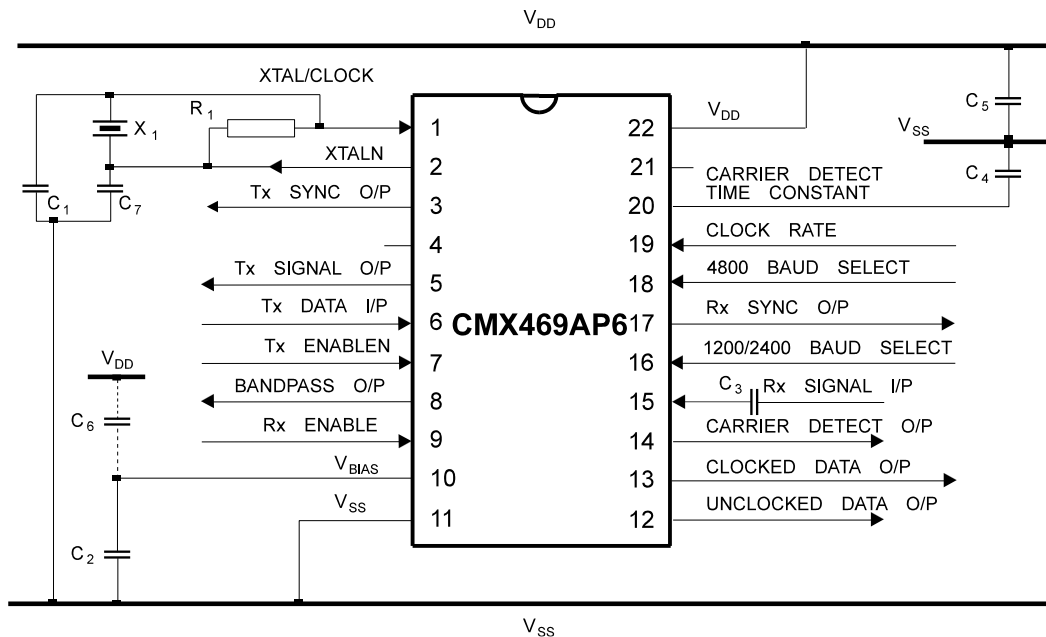
### 1.3 Signal List

CMX469A		Signal		Description
D3	E2	Name	Type	
Pin No.	Pin No.	Name	Type	
1	1	CLOCK/XTAL	I/P	The input to the on-chip inverter, for use with either a 1.008MHz or a 4.032MHz Xtal or an external clock. Clock frequency selection is by means of the CLOCK RATE pin. This affects the operational data rate of the device. Operation of any CML microcircuit without a Xtal or clock input may cause device damage.
2	2	XTALN	O/P	The output of the on-chip inverter.
3	3	Tx SYNC O/P	O/P	A squarewave, produced on-chip, to synchronize the input of logic data and transmission of the FFSK/MSK signal.
4	5	Tx SIGNAL O/P	O/P	When the transmitter is enabled, this pin outputs the FFSK/MSK signal. With the transmitter disabled, this pin is set to a high-impedance state.
5	7	Tx DATA I/P	I/P	The serial logic data to be transmitted is input to this pin.
6	8	Tx ENABLEN	I/P	A logic '0' will enable the transmitter. A logic '1' at this input will put the transmitter into powersave whilst forcing Tx SYNC OUTPUT to a logic '1' and Tx SIGNAL OUTPUT to a high-impedance state. This pin is internally pulled to V <sub>DD</sub> .
7	9	BANDPASS O/P	O/P	The output of the Rx Bandpass Filter. This output impedance is typically 10k $\Omega$ and may require buffering prior to use.
8	10	Rx ENABLE	I/P	The control of the Rx function
9	11	V <sub>BIAS</sub>	BI	The output of the on-chip analogue bias circuitry. Held internally at V <sub>DD</sub> /2, this pin should be decoupled to V <sub>SS</sub> by a capacitor (C2). This bias voltage is maintained under all powersave conditions.
10	12	V <sub>SS</sub>	PWR	Negative supply rail (GND).
11	13	UNCLOCKED DATA O/P	O/P	The recovered asynchronous serial data output from the receiver.
12	14	CLOCKED DATA O/P	O/P	The recovered synchronous serial data output from the receiver. Data is latched out by the recovered clock, available at the Rx SYNC O/P.

CMX469A		Signal		Description
D3	E2	Name	Type	
Pin No.	Pin No.	Name	Type	
13	15	CARRIER DETECT O/P	O/P	When an FFSK/MSK signal is being received this output is a logic '1'.
14	16	Rx SIGNAL I/P	I/P	The FFSK/MSK signal input for the receiver. This input should be coupled via a capacitor, C3.
15	18	Rx SYNC O/P	O/P	A flywheel squarewave output. This clock will synchronize to incoming Rx FFSK/MSK data.
16	19	1200/2400 BAUD SELECT	I/P	A logic '1' on this pin selects the 1200 baud option. Tone frequencies are: one cycle of 1200Hz represents a logic '1,' one-and-a-half cycles of 1800Hz represents a logic '0.'  A logic '0' on this pin selects the 2400 baud option. Tone frequencies are: one-half cycle of 1200Hz represents a logic '1,' one cycle of 2400Hz represents a logic '0.' This function is also used, in part, to select the 4800 baud option. This pin has an internal 1M $\Omega$ pullup resistor.
17	20	4800 BAUD SELECT	I/P	A logic '1' on this pin combined with a logic '0' on the 1200/2400 BAUD SELECT pin will select the 4800 baud option (1M $\Omega$ pulldown resistor). Tone frequencies are: one-half cycle of 2400Hz represents a logic '1,' one cycle of 4800Hz represents a logic '0.' Operation at 4800 baud is only achieved by using a 4.032MHz Xtal or clock.
18	21	CLOCK RATE	I/P	A logic input to select and allow the use of either a 1.008MHz or 4.032MHz Xtal/clock. Logic '1' = 4.032MHz, logic '0' = 1.008MHz. This input has an internal pulldown resistor (1.008MHz).
19	22	CARRIER DETECT TIME CONSTANT	BI	Part of the carrier detect integration function. The value of C4 connected to this pin will affect the carrier detect response time and hence noise performance.
20	24	VDD	PWR	Positive supply rail. A single 2.7 to 5.0 volt supply is required. This pin should be decoupled to VSS by a capacitor (C5).  No internal connection, do not use.
	4, 6, 17, 23			

**Notes:** I/P = Input O/P = Output BI = Bidirectional PWR = Power

## 1.4 External Components



Component	Value
R1	1.0M $\Omega$
C1	33.0pF
C2	1.0 $\mu$ F
C3	0.1 $\mu$ F
C4	0.1 $\mu$ F
C5	1.0 $\mu$ F
C6	1.0 $\mu$ F
C7	33.0pF
X1	1.008MHz or 4.032MHz

### Notes:

1. VBIAS may be decoupled to VSS and VDD using C2 and C6 when input signals are referenced to the VBIAS pin. For input signals referenced to VSS, decouple VBIAS to VSS using C2 only.
2. The performance of the Carrier Detect function will be affected by the nature of the noise spectrum in the received channel. The value of C4 determines the Carrier Detect Time Constant. A long time constant results in improved noise immunity but increased response time. C4 may be varied to trade-off response time for noise immunity.
3. A 4.032MHz Xtal/clock is required for 4800 Baud operation.

**Figure 2 Recommended External Components**

## 1.5 General Description

The CMX469A has two sections, apart from the Xtal oscillator circuit and clock dividers. These sections may be independently powersaved.

### **Transmitter**

The transmitter is enabled by taking Tx EnableN low. Serial data applied to Tx Data Input is sampled internally and an FFSK/MSK sequence is generated. After filtering, this is output at Tx Signal O/P and the transmit clock derived from this signal is output at Tx Sync O/P.

### **Receiver**

The receiver is enabled by taking Rx Enable high. The signal applied to Rx Signal I/P is filtered and recovered as serial data from the Unclocked Data O/P. A flywheel synchroniser is used to extract a clock from the recovered serial data stream. The clock is available at Rx Sync O/P and the retimed serial data is available at Clocked Data O/P.

The integrated peak values of the Rx amplitude are compared with out-of-band noise levels and used to make a signal-to-noise assessment, which is available at Carrier Detect O/P.

A Bandpass O/P is also available from the output of the first Rx filter stage, but will require buffering before use.

## 1.6 Application Notes

### 1.6.1 Rx Enable

The control of the relevant outputs with reference to the Rx Enable input is described below:

Rx Enable	Rx Function	Clock Data O/P	Carrier Detect O/P	Rx Sync Out
'1'	Enabled	Enabled	Enabled	Enabled
'0'	Powersave	'0'	'1' or '0'	'1' or '0'

After enabling the Receiver, a time of at least 8 bit periods plus 2ms should be allowed for the Carrier Detect circuit to stabilise and give a valid output.

### 1.6.2 Operational Data Rate Configurations

Operational Data Rate Configurations are as described below:

Xtal/Clock Frequency	1.008MHz			4.032MHz		
Clock Rate	'0'		'0'	'1'	'1'	'1'
1200/2400 Select	'1'		'0'	'1'	'0'	'0'
4800 Select	'0'		'0'	'0'	'0'	'1'
Baud Rate	1200		2400	1200	2400	4800

### 1.6.3 Test Set Up

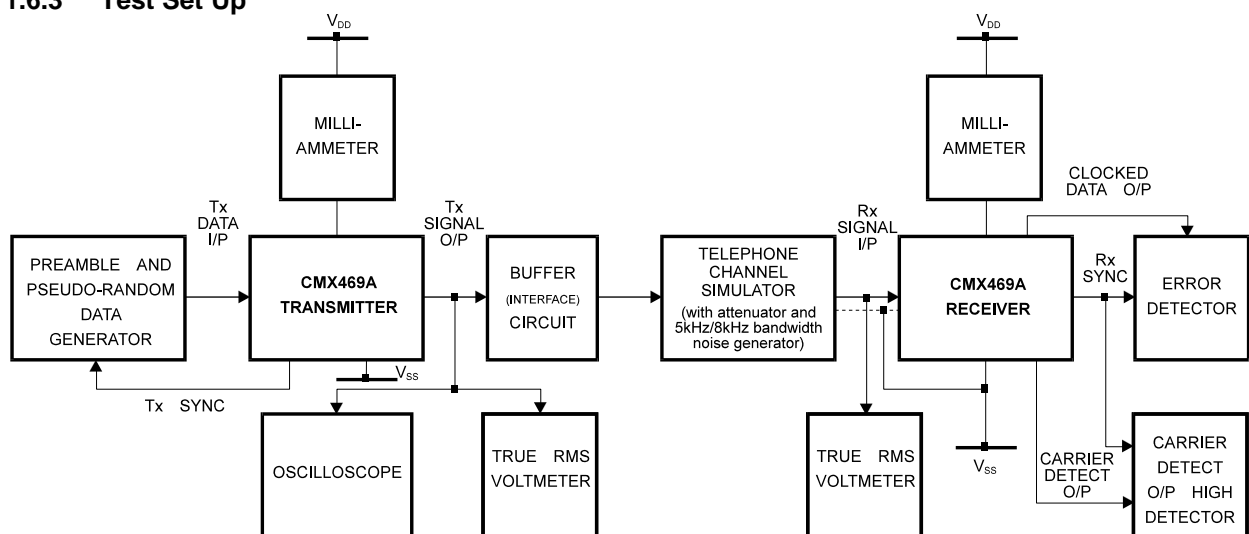


Figure 3 Suggested CMX469A Test Set-Up

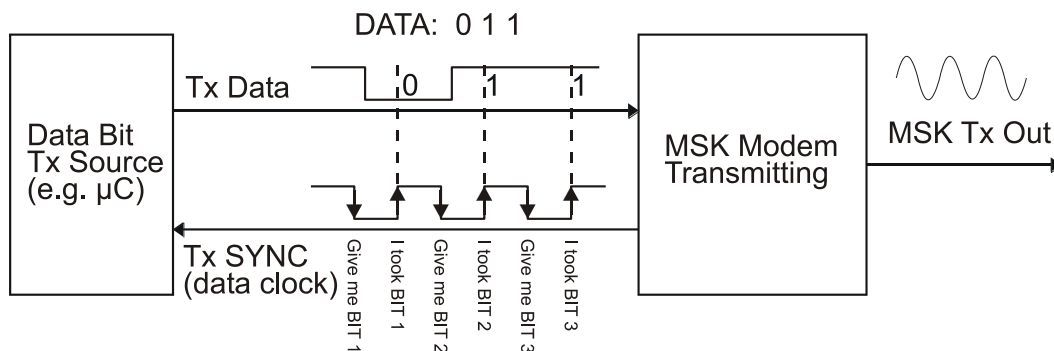


#### 1.6.4 Synchronous Modem Design Considerations

The CMX469A is an easily applied data pump which can be used with many protocols. Because it is an MSK (minimum shift keying) modem, it achieves a more noise resistant, higher data rate in a narrower bandwidth than other FSK (frequency shift keying) modems. This characteristic is especially important for wireless applications because it fundamentally determines the bandwidth of RF transmissions, which are strictly limited and controlled by regulatory agencies. Using MSK signalling, the CMX469A data modem can achieve a 2400 bps data rate within the typical 300-3000 Hz voice band of many common radios.

In order to achieve this advantage, an MSK modem must precisely control the bit rate and timing of the modulated Tx output signal bits. This control is asserted by the MSK modem with a data clock signal which is output by the modem to pace the Tx data source (e.g. a microcontroller). The data clock signal, in effect, indicates when the Tx data source should provide the next Tx data bit to the modem. See Figure 4. Because this type of interface involves the use of a modem-generated bit clock signal to control the timing of when new Tx data bits must be supplied from the data source, the interface is called synchronous.

Another characteristic of a synchronous modem is that, to receive data, it must first learn the data bit timing of the Rx signal stream before it can accurately demodulate Rx data bits. Accordingly, a synchronous modem undergoes a period of training or synchronisation when it first begins to receive a stream of MSK-modulated signal. During this initial receive phase, the received signal is evaluated over several bit times as the modem 'locks-on' and achieves proper receive synchronisation. This training sequence, called a preamble, is a specific data pattern which must be added to the 'front' of a transmit data stream with the start of each new transmission. A specific preamble data pattern (e.g. 16 bits of alternating 0101 .... for the CMX469A) is used to optimise the training accuracy while minimising the number of preamble bits required.



**Figure 4 Synchronous Transmit Operation**

Non-synchronous or asynchronous interfaces are commonly found in wired applications which do not have the bandwidth efficiency requirements of wireless systems. A well-known example is the serial port of a personal computer, which can transmit a 1200 bps (or faster) data signal without using an additional data clock signal to control the precise rate and timing of data bits being transmitted to a typical telephone line modem. This is achieved by preceding the sequence of data bits with a START bit and terminating the sequence of data bits with a STOP bit. The timing of the Rx signal stream can be determined by examining the duration of the START bit to a sufficient accuracy for the reception of a short (usually 8 or 9 bit) sequence of data bits. Popular modem standards, such as ITU V.23 and Bell 202, use FSK signalling to pass such asynchronous serial port data signals over telephone systems.

Another aspect of asynchronous interfaces and modems is that they can carry data streams which are not at the exact, nominal data rate. For example, a 1200 bps FSK modem will typically operate properly when supplied with transmit data streams of 1194 to 1206 bps.

Because of the differences in synchronous and asynchronous interfaces, they cannot successfully operate if directly connected. In other words, a personal computer's RS232 serial port cannot directly interface to an MSK modem. This is because:

- The asynchronous interface may provide data bits too fast or too slow compared to the precise rate required for MSK signalling (a bit rate, or pacing, incompatibility).
- The timing of each specific data bit presented by an asynchronous interface will not be aligned with the precise bit timing required for MSK signalling (a bit timing incompatibility).

Synchronous and asynchronous interfaces can be successfully interconnected for applications requiring the advantages of both. This typically involves the use of data buffering and retiming circuits to resolve the timing and pacing issues.

## 1.7 Performance Specification

### 1.7.1 Electrical Performance

#### Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply ( $V_{DD} - V_{SS}$ )	-0.3	7.0	V
Voltage on any pin to $V_{SS}$	-0.3	$V_{DD} + 0.3$	V
Current into or out of $V_{DD}$ and $V_{SS}$ pins	-30	+30	mA
Current into or out of any other pin	-20	+20	mA

<b>D3 Package</b>	Min.	Max.	Units
Total Allowable Power Dissipation at $T_{amb} = 25^{\circ}\text{C}$		560	mW
... Derating		5.6	mW/ $^{\circ}\text{C}$
Storage Temperature	-55	+125	$^{\circ}\text{C}$
Operating Temperature	-40	+85	$^{\circ}\text{C}$

<b>E2 Package</b>	Min.	Max.	Units
Total Allowable Power Dissipation at $T_{amb} = 25^{\circ}\text{C}$		1000	mW
... Derating		10.0	mW/ $^{\circ}\text{C}$
Storage Temperature	-55	+125	$^{\circ}\text{C}$
Operating Temperature	-40	+85	$^{\circ}\text{C}$

## Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply ( $V_{DD} - V_{SS}$ )		2.7	5.5	V
Operating Temperature		-40	+85	°C
Xtal Frequency	1	4.028	4.036	MHz

Note 1: A Xtal frequency of 1.008MHz (1200/2400 baud only) or 4.032MHz is required for correct operation. A frequency tolerance of  $\pm 0.1\%$  is recommended, but ultimately the tolerance selected will depend upon system requirements.

## Operating Characteristics

For the following conditions unless otherwise specified:

$V_{DD} = 2.7V$  at  $T_{amb} = 25^{\circ}C$  and  $V_{DD} = 3.0V$  to  $5.5V$  at  $T_{amb} = -40^{\circ}C$  to  $+85^{\circ}C$ ,  
Xtal/Clock Frequency = 4.032MHz, Bit Rate = 1200 baud, Rx Input Level = 300mVrms.

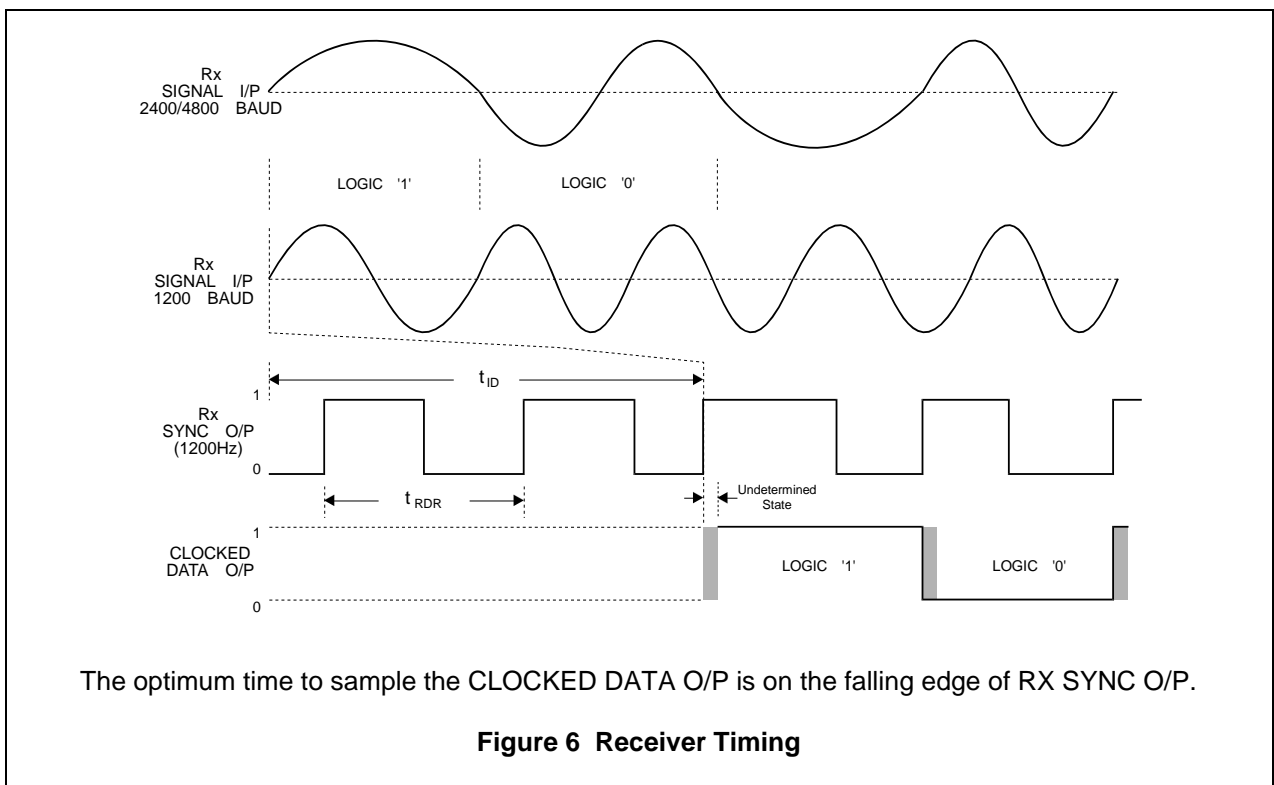
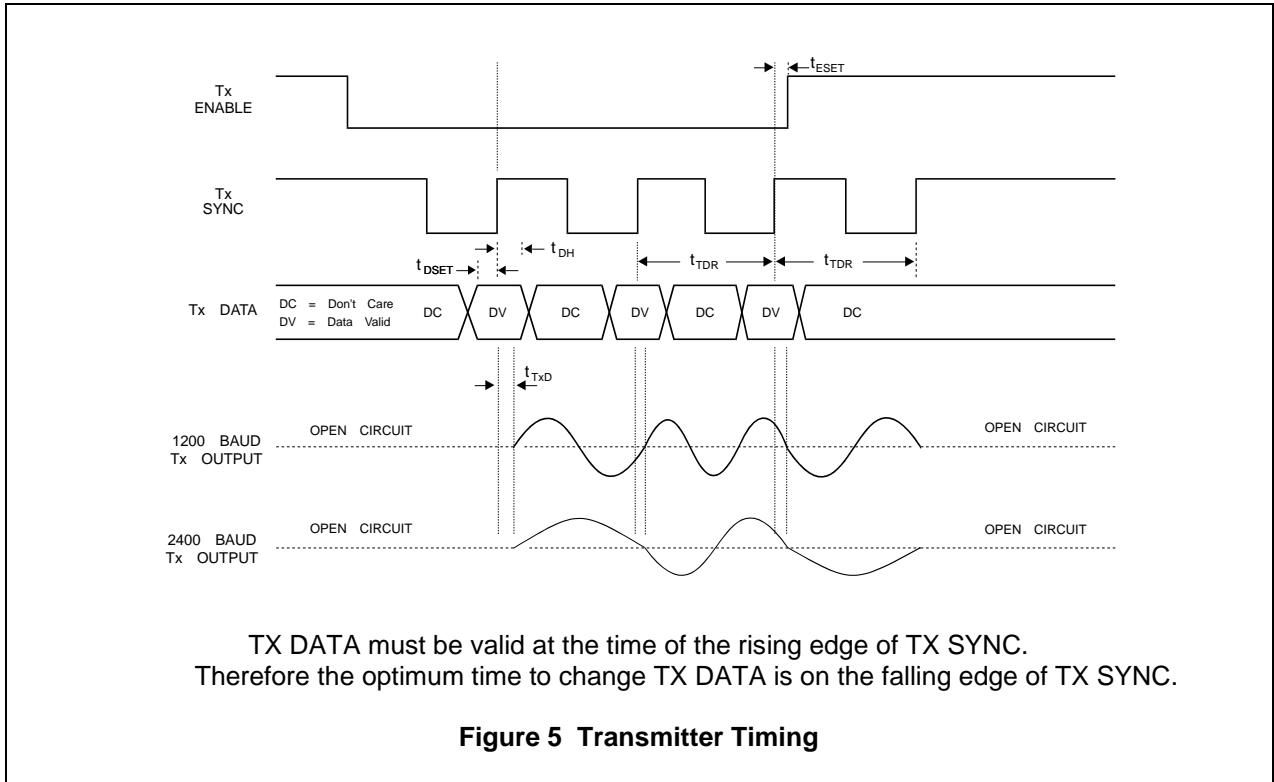
	Notes	Min.	Typ.	Max.	Units
<b>Static Values</b>					
$I_{DD}$ Rx Enabled, Tx Disabled ( $V_{DD} = 5.0V$ )	2	-	3.6	-	mA
$I_{DD}$ Rx and Tx Enabled ( $V_{DD} = 5.0V$ )	2	-	4.5	-	mA
$I_{DD}$ Rx and Tx Disabled ( $V_{DD} = 5.0V$ )	2	-	650	-	$\mu A$
$I_{DD}$ Rx Enabled, Tx Disabled ( $V_{DD} = 3.0V$ )	2	-	1.5	-	mA
$I_{DD}$ Rx and Tx Enabled ( $V_{DD} = 3.0V$ )	2	-	2.0	-	mA
$I_{DD}$ Rx and Tx Disabled ( $V_{DD} = 3.0V$ )	2	-	300	-	$\mu A$
Logic '1' Level	1	70%	-	-	$V_{DD}$
Logic '0' Level	1	-	-	30%	$V_{DD}$
Digital Output Impedance		-	4.0	-	k $\Omega$
Analogue and Digital Input Impedance		100	-	-	k $\Omega$
Tx Output Impedance ( $V_{DD} = 5.0V$ )		-	0.6	1.0	k $\Omega$
<b>Dynamic Values</b>					
<b>Receiver</b>					
Signal Input Dynamic Range SNR = 50dB	3, 4	100	230	1000	mVrms
Bit Error Rate at SNR = 12dB	4, 5				
1200 Baud		-	2.5	-	$10^{-4}$
2400 Baud		-	1.5	-	$10^{-3}$
4800 Baud		-	1.5	-	$10^{-3}$
Bit Error Rate at SNR = 20dB	4, 5				
1200/2400/4800 Baud		-	<1.0	-	$10^{-8}$
Receiver Synchronization at SNR = 12dB probability of bit 16 being correct	7	-	0.995	-	

	Notes	Min.	Typ.	Max.	Units
<b>Carrier Detect</b>					
Sensitivity	3 1, 7, 8	-	-	150	mVrms
Probability of CD being High after bit 16: with SNR = 12dB	9		0.995		
with 230mVrms Noise and No Signal	9		0.05		
<b>Transmitter Output</b>					
Tx Output Level	1	-	775	-	mVrms
Output Level Variation for 1200/1800Hz or 1200/2400Hz or 2400/4800Hz		0	-	+/-1.0	dB
Output Distortion	10	-	3.0	5.0	%
3rd Harmonic Distortion	10	-	2.0	3.0	%
Isochronous Distortion					
1200Hz - 1800Hz/1800Hz - 1200Hz		-	25.0	40.0	µs
1200Hz - 2400Hz/2400Hz - 1200Hz		-	20.0	30.0	µs
2400Hz - 4800Hz/4800Hz - 2400Hz		-	10.0	20.0	µs
Logic '1' Carrier Frequency 1200 Baud	6	-	1200	-	Hz
2400 Baud	6	-	1200	-	Hz
4800 Baud	6	-	2400	-	Hz
Logic '0' Carrier Frequency 1200 Baud	6	-	1800	-	Hz
2400 Baud	6	-	2400	-	Hz
4800 Baud	6	-	4800	-	Hz

**Notes:**

1. Measured at  $V_{DD} = 5.0$  volts. Signal levels and thresholds are proportional to  $V_{DD}$ .
2. Excludes any current drawn by external components, but includes current drawn by the crystal components.
3. See Figure 7 (Typical Variation of BER with Input Signal Level).
4. SNR = Signal-to-Noise Ratio in the Bit-Rate Bandwidth.
5. See Figure 8 (Typical Rx BER vs Signal-to-Noise Ratio).
6. Dependent upon Xtal tolerance.
7. With an alternating (1010...) pattern.
8. Measured with a 150mVrms input signal (no noise).
9. A signal level of 230mVrms is used in C.D. probability measurements. Noise bandwidth is 5kHz (1200/2400 baud operation) or 8kHz (4800 baud operation). See Section 1.4, Note 2 for details on optimising noise immunity.
10. For an unmodulated carrier.

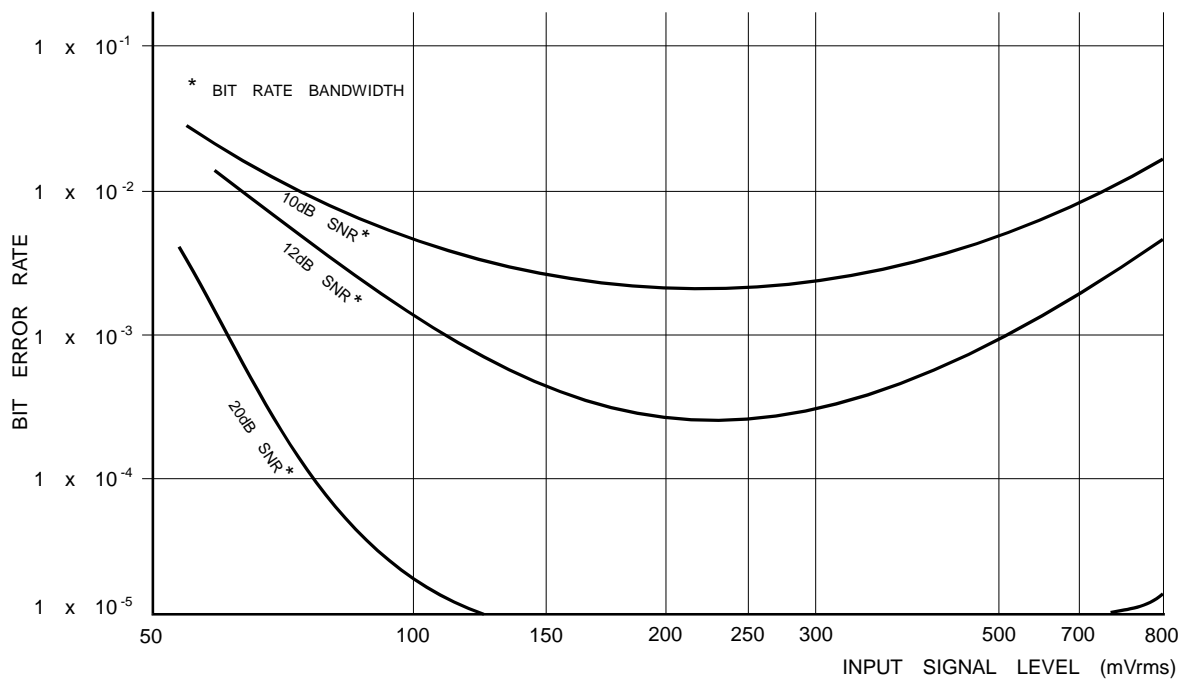
**Interface Timing Diagrams**



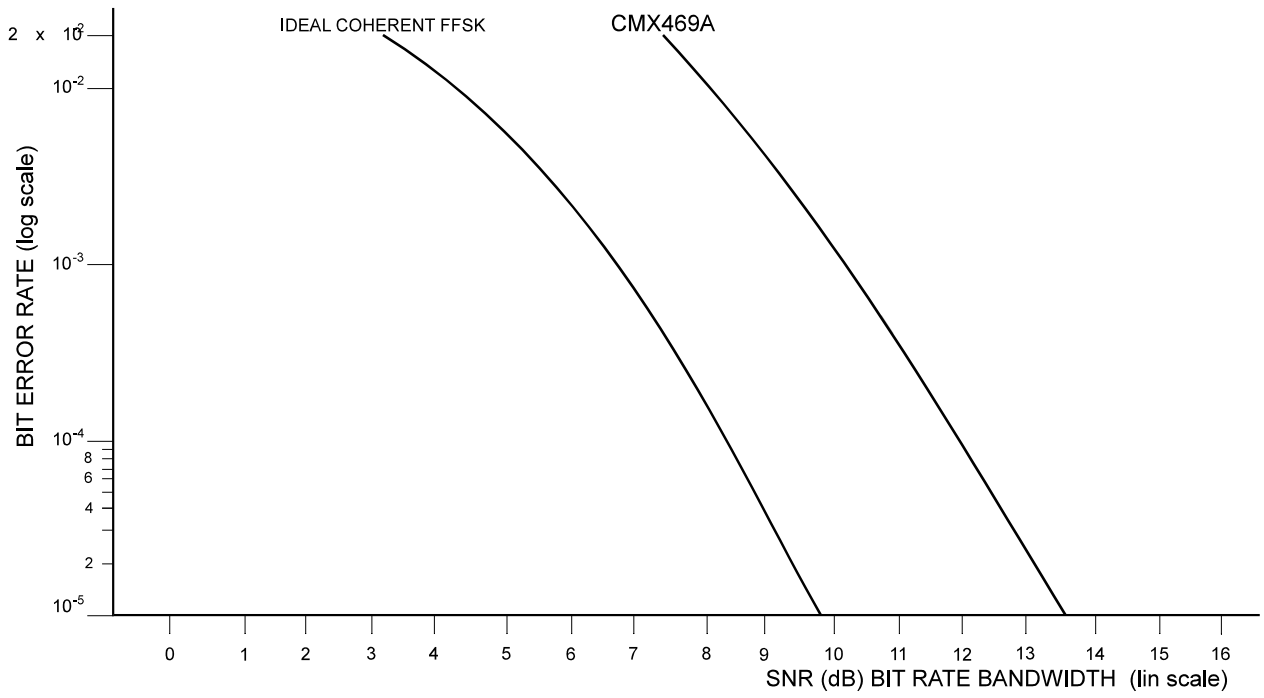
### 1.7.1 Electrical Performance (continued)

	Interface Timings	Notes	Min.	Typ.	Max.	Units
$t_{\text{ESET}}$	Tx Delay, Signal to Disable Time	2	2.0	-	800	$\mu\text{s}$
$t_{\text{DSET}}$	Data Set-Up Time	1	2.0	-	-	$\mu\text{s}$
$t_{\text{DH}}$	Data Hold Time		2.0	-	-	$\mu\text{s}$
$t_{\text{TXD}}$	Tx Delay to O/P Time		-	1.2	-	$\mu\text{s}$
$t_{\text{TDR}}$	Tx Data Rate Period	2	-	833	-	$\mu\text{s}$
$t_{\text{RDR}}$	Rx Data Rate Period	2	800	-	865	$\mu\text{s}$
	Undetermined State (see Figure 6)		-	-	2.0	$\mu\text{s}$
$t_{\text{ID}}$	Internal Rx Delay		-	1.5	-	ms

- Notes:**
1. Consider the Xtal/Clock tolerance.
  2. 1200 Baud example.



**Figure 7 Typical Variation of Bit Error Rate with Input Level**



**Figure 8 Typical Rx Bit Error Rate vs Signal-to-Noise Ratio**



1.7.2 Packaging

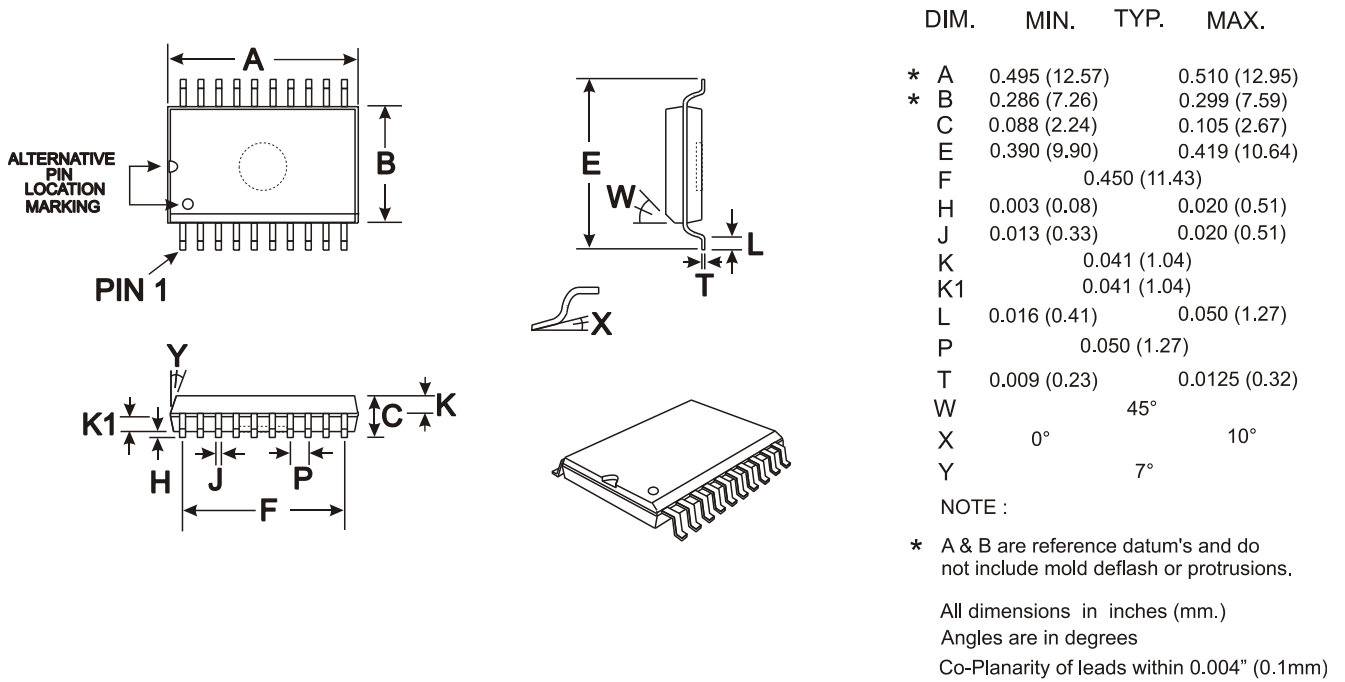


Figure 9 D3 Mechanical Outline: Order as part no. CMX469AD3

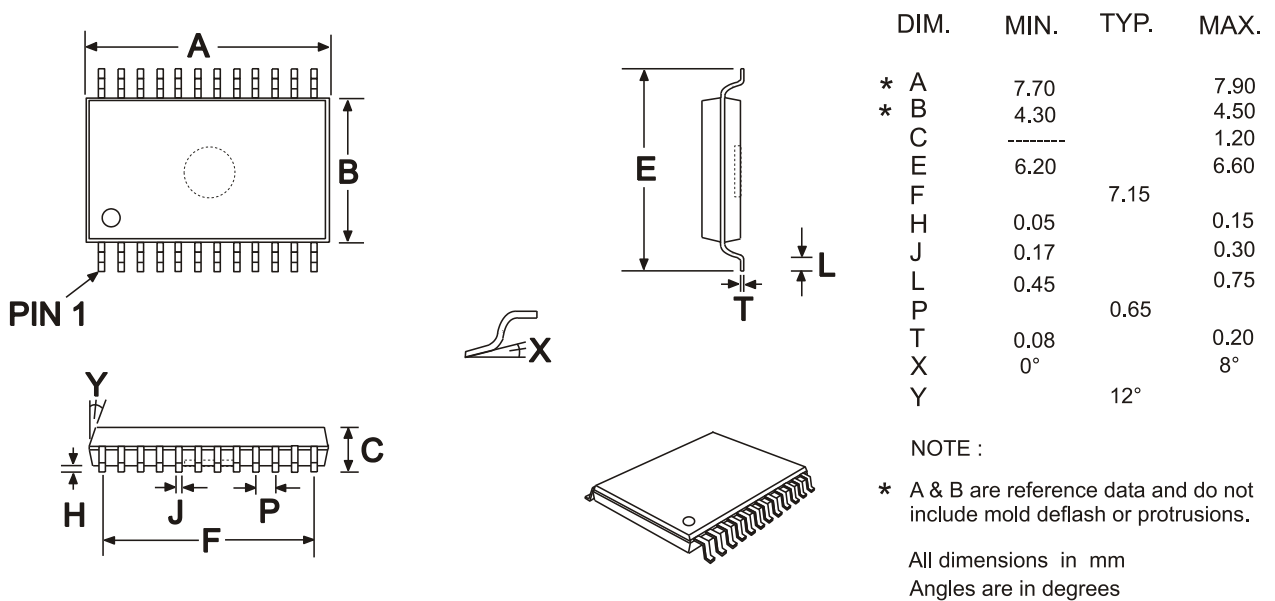


Figure 10 E2 Mechanical Outline: Order as part no. CMX469AE2

Handling precautions: This product includes input protection, however, precautions should be taken to prevent device damage from electro-static discharge. CML does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. CML reserves the right at any time without notice to change the said circuitry and this product specification. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with this product specification. Specific testing of all circuit parameters is not necessarily performed.



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